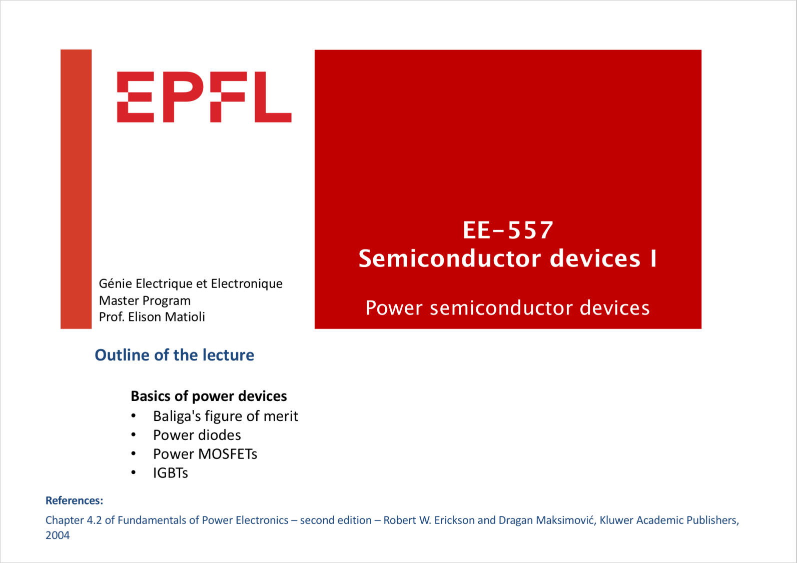
Course 24 v2

Monday, 9 December 2024 14:48

EE557 Cours 24 - Power...



Génie Electrique et Electronique
Master Program
Prof. Elison Matioli

EE-557
Semiconductor devices I

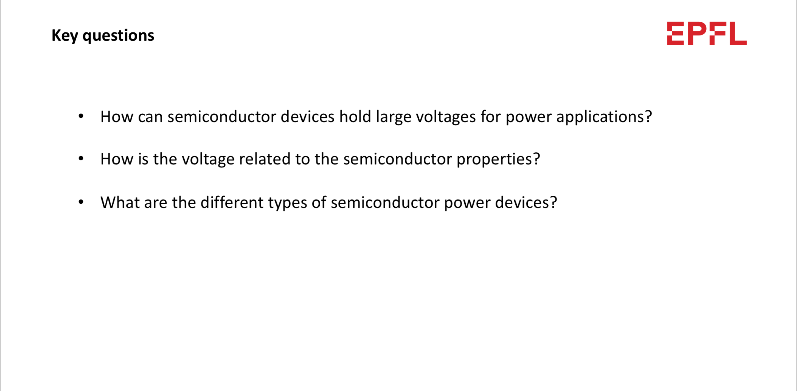
Power semiconductor devices

Outline of the lecture

Basics of power devices
- Baliga's figure of merit
- Power diodes
- Power MOSFETs
- IGBTs

References:

Chapter 4.2 of Fundamentals of Power Electronics – second edition – Robert W. Erickson and Dragan Maksimović, Kluwer Academic Publishers, 2004

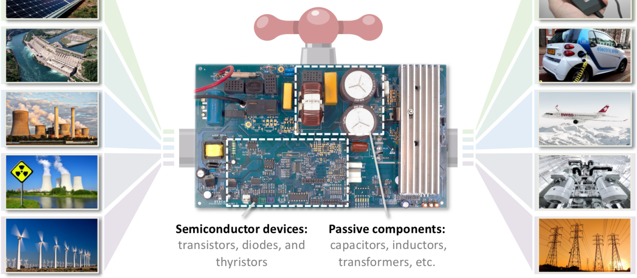


Key questions

- How can semiconductor devices hold large voltages for power applications?
- How is the voltage related to the semiconductor properties?
- What are the different types of semiconductor power devices?

Introduction to power electronics

Power Electronics

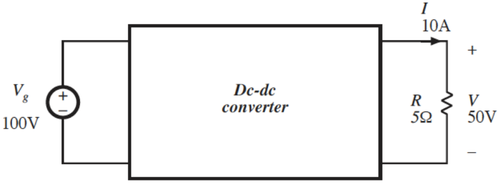


Semiconductor devices: transistors, diodes, and thyristors

Passive components: capacitors, inductors, transformers, etc.

Introduction to power electronics

DC-DC converter

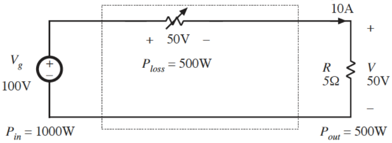


I
10A
+
V_g
100V
Dc-dc converter
R
5Ω
V
50V
–

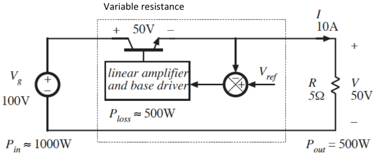
How can such converter be realised?

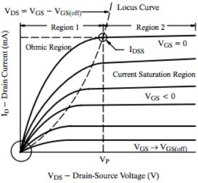
Principles of power conversion

Solution 1: voltage divider


I
10A
+ 50V –
P_{loss} = 500W
V_g
100V
R
5Ω
+
V
50V
–
P_{in} = 1000W
P_{out} = 500W

Solution 2: linear amplifier

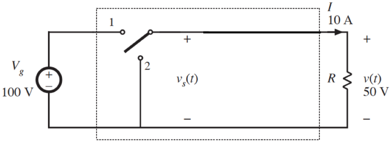

Variable resistance
+ 50V –
I
10A
linear amplifier and base driver
V_{ref}
V_g
100V
R
5Ω
+
V
50V
–
P_{loss} ≈ 500W
P_{in} ≈ 1000W
P_{out} = 500W

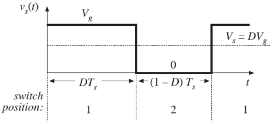


These are very inefficient solutions

Principles of power conversion

Concept of switching


1
2
I
10 A
+
$v_s(t)$
–
V_g
100 V
R
+
$v(t)$
50 V
–



D = switch duty cycle
$0 \le D \le 1$

T_s = switching period

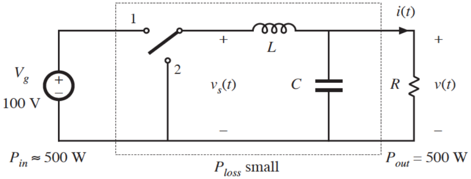
f_s = switching frequency
$= 1 / T_s$

DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = DV_g$$

Principles of power conversion

Addition of (ideally lossless) *L*-*C* low-pass filter, for removal of switching harmonics:

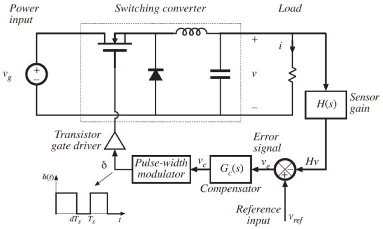

1
2
$i(t)$
+
L
V_g
100 V
$v_s(t)$
C
R
$v(t)$
–
$P_{in} \approx 500$ W
P_{loss} small
$P_{out} = 500$ W

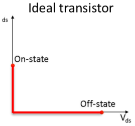
- Cut-off frequency of the filter must be much smaller that the switching frequency **f_0 << f_S**
- This is called a **buck converter: $V_{out} = DV_{in}$**

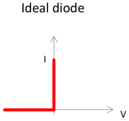
Principles of power conversion

Realization of such circuit:

Power transistors + power diodes + filters + circuit de regulation


Power input
Switching converter
Load
v_g
+
–
i
v
$H(s)$
Sensor gain
Transistor gate driver
δ
δ(t)
dT_s
T_s
t
Pulse-width modulator
v_c
$G_c(s)$
Compensator
v_e
Error signal
Hv
Reference input
v_{ref}





Product V x I must be as close as possible to zero

Power transistors and diodes are the heart of power converters

They are power switching devices, which:

Should **conduct with small losses**, **switch fast** with small losses, **hold large voltages**

Efficient conversion is the goal: what are the loss mechanisms?

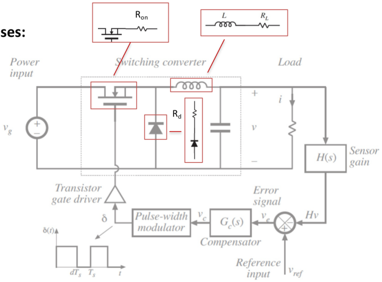
Fundamentals of Power Electronics, Robert W. Erickson, Dragan Maksimović

Efficiency

Two main loss mechanisms:

1. **Conduction losses:** when devices are conducting
   - Semiconductor forward bias
   - Parasitics: inductances, capacitances, resistances
2. **Switching losses:** when devices are switching

1. Conduction losses:

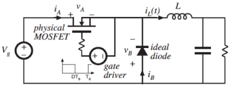

R_{on}
L
R_L
Power input
Switching converter
Load
v_g
R_d
+
i
v
–
$H(s)$
Sensor gain
Transistor gate driver
Error signal
δ
Pulse-width modulator
v_c
$G_c(s)$
v_e
Hv
$\delta(t)$
Compensator
Reference input
v_{ref}
dT_s
T_s
t

Dissipated power

$P_{conduction} = R_{on} I_{RMS}^2$

Efficiency

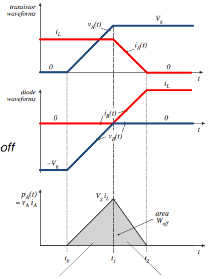
2. Switching losses:


i_A
v_A
+
–
$i_L(t)$
L
physical MOSFET
V_g
v_B
ideal diode
gate driver
i_B
DT_s
T_s

Buck converter example

$$v_B(t) = v_A(t) - V_g$$
$$i_A(t) + i_B(t) = i_L$$

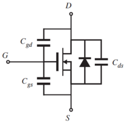
transistor turn-off transition



Charging time of C_{GD}

Discharging time of C_{GS}

Equivalent circuit


D
C_{gd}
G
C_{ds}
C_{gs}
S

Energy lost during transistor turn-off transition:

$$W_{off} = \tfrac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

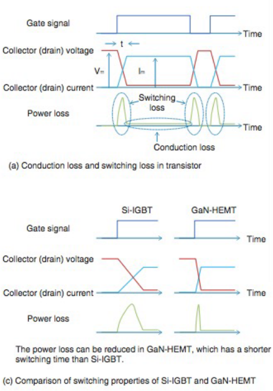
Similar result during transistor turn-on transition.
Average power loss:

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching}\\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

Switching losses are proportional to the switching frequency…

…while conduction losses are fixed

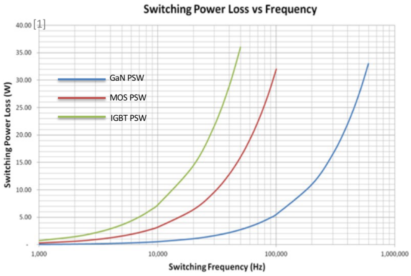
Switching losses


Gate signal
Time
Collector (drain) voltage
t
Vm
Im
Collector (drain) current
Time
Switching loss
Power loss
Time
Conduction loss
Si-IGBT
GaN-HEMT
Gate signal
Time
Collector (drain) voltage
Collector (drain) current
Time
Power loss

(a) Conduction loss and switching loss in transistor

The power loss can be reduced in GaN-HEMT, which has a shorter switching time than Si-IGBT.

(c) Comparison of switching properties of Si-IGBT and GaN-HEMT



Switching losses are proportional to the switching frequency: Fast devices are required!

[1] http://pi-innovo.com/content/uploads/2016/03/Figure-2.png

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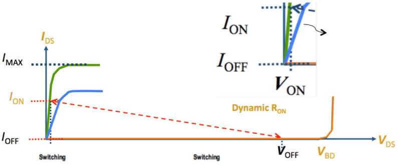
Requirements for efficient power electronic devices

Power switch:

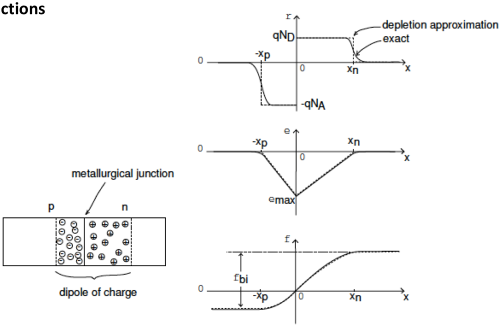


It operates in two regimes:
ON: Low voltage, high current
OFF: High voltage, low current

- High breakdown voltage
- Low on-resistance: Small on-state power dissipation: $I_{rms}^2 x R_{on}$
- High maximum current
- Low leakage current at breakdown voltage: Small off-state power dissipation: $I_{off} x V_{br}$

How to get large breakdown voltages?

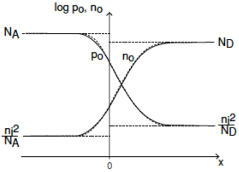
Back to pn junctions


r
qND
depletion approximation
exact
0
-xp
0
xn
x
-qNA
e
0
-xp
xn
0
x
emax
metallurgical junction
p
n
dipole of charge
f
fbi
0
-xp
0
xn
x

Distinct regions:
Around metallurgical junction:
space charge region (SCR)

Far from junction:
quasi-neutral regions (QNR)
ρ ~ 0

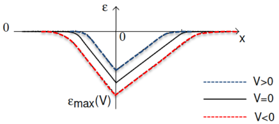
Electric field is constant and equal to zero

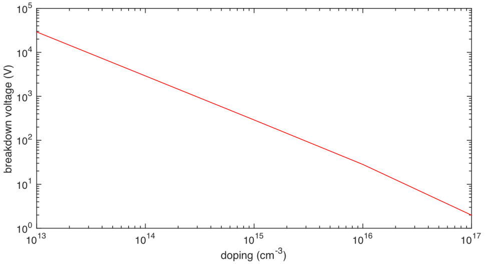


Ideal p-n junction out of equilibrium

Peak electric field:

$$|\mathcal{E}_{max}(V)| = \sqrt{\frac{2qN_AN_D(\phi_{bi}-V)}{\epsilon(N_D+N_A)}} = |\mathcal{E}_{max}(V=0)|\sqrt{1-\frac{V}{\phi_{bi}}}$$





How to make a power device?

Power diodes

Goal:

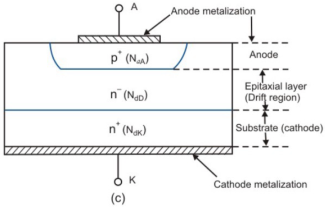
Conduct **several kilo amps** of current in the forward direction with very **little power loss** while blocking **several kilo volts** in the reverse direction.

Large blocking voltage requires **wide depletion layer** in order to restrict the maximum electric field strength below the breakdown voltage (impact ionization level).

Space **charge density in the depletion layer should also be low** in order to yield a wide depletion layer for a given **maximum electric field strength**.

This is satisfied in a **lightly doped p-n junction** diode **of sufficient width** to accommodate the required depletion layer.

PIN diode


A
Anode metalization
p+ (NaA)
Anode
Epitaxial layer
(Drift region)
n− (NdD)
n+ (NdK)
Substrate (cathode)
K
Cathode metalization
(c)

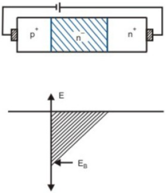
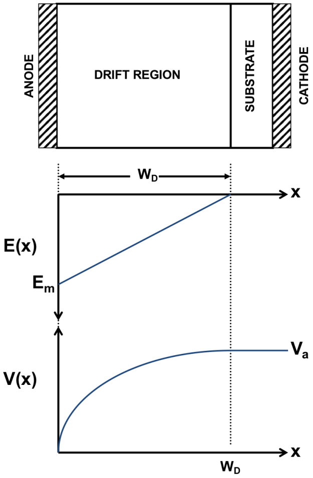


Figure of merit: how to compare different semiconductors


ANODE
DRIFT REGION
SUBSTRATE
CATHODE
WD
x
E(x)
Em
V(x)
Va
x
WD

Specific on-resistance (Ωcm²)

$$R_{ON,SP} = \frac{W_D}{qN_D\mu_n}$$

$$V = \frac{E_m W_D}{2} \quad \text{thus} \quad \boxed{W_D = \frac{2BV}{E_C}}$$

Poisson's Equation:

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_S} = -\frac{qN_D}{\varepsilon_S}$$

$$E(x) = -\frac{qN_D}{\varepsilon_S}(W_D - x)$$

$$V(x) = \frac{qN_D}{\varepsilon_S}\left(W_D x - \frac{x^2}{2}\right)$$

$$V_a = \frac{qN_D W_D^2}{2\varepsilon_S} \qquad \boxed{N_D = \frac{\varepsilon_S E_C^2}{2qBV}}$$

Figure of merit: how to compare different semiconductors

Ideal Specific On-Resistance ($R_{ON,SP}$):

$$W_D = \frac{2BV}{E_C} \quad \text{and} \quad N_D = \frac{\varepsilon_S E_C^2}{2qBV}$$

Baliga's figure of merit

$$R_{ON,SP} = \frac{W_D}{q\mu_n N_D}$$

$$\boxed{R_{ON,SP} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3}}$$

$R_{on,sp}$ is related to material properties

$$\boxed{BFOM = \varepsilon_S \mu_n E_C^3 = \frac{4BV^2}{R_{ON,SP}}}$$

Critical electric field E_c is very important, followed by mobility in the drift layer

B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer 2008

Wide-band-gap materials

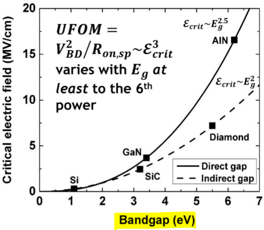
$$\boxed{R_{ON,SP} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3}}$$

$R_{on,sp}$ is related to material properties

Baliga's figure of merit

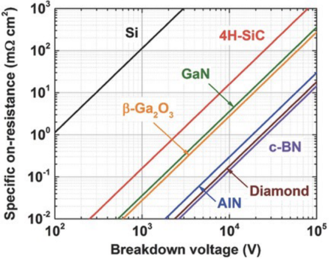
$$\boxed{BFOM = \varepsilon_S \mu_n E_C^3 = \frac{4BV^2}{R_{ON,SP}}}$$

Relationship between Ec and Eg



Hudgins et al., IEEE Trans. on Pow. Elec. 18, 3 (2003),
Tsao et al., Advanced Elec. Mat. 4, 1600501 (2018)

BFOM for different materials



Influence of material properties

Parameter	Silicon	4H-SiC	GaN	Diamond
E_g, eV	1.12	3.26	3.39	5.47
E_{crit}, MV/cm	0.23	2.2	3.3	5.6
ε_r	11.8	9.7	9.0	5.7
μ_n, cm^2/V·s	1400	950	800/1700[b]	1800
BFoM[a] relative to Si	1	500	1300/2700[b]	9000
n_i, cm^{-3}	$1\cdot10^{10}$	$8\cdot10^{-9}$	$2\cdot10^{-10}$	$1\cdot10^{-20}$
λ, W/cm·K	1.5	3.8	1.3/3[c]	20

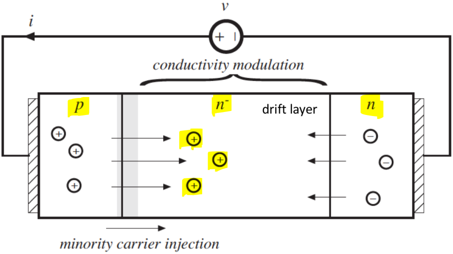
Desired properties, found in some of these wide band-gap materials:

- Higher breakdown strength: same breakdown voltage with less material
- Higher switching speed: lower switching losses
- Lower losses: enables significantly reduced volume and decreased cooling requirements
- Higher frequency: smaller passive components (inductors and capacitors)

Power diodes

diode PIN

Forward polarization


v
i
+
conductivity modulation
p
n^-
drift layer
n
minority carrier injection

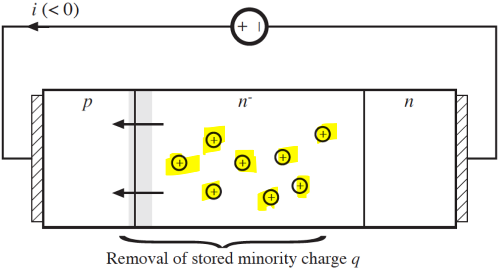
Forward polarization:

- Injection of minority carriers in the drift layer: conductivity modulation
- Charges are accumulated in the region «i»:
  - Resistance is reduced
  - But slows down the device
- Minority carrier device

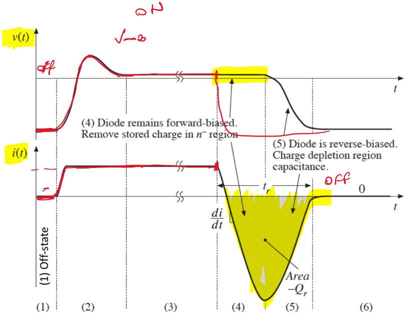
Power diodes

Turn-off transient

v


$i\,(<0)$
+ |
p
n^-
n
Removal of stored minority charge q

Power diodes



(4) Reduction of the stored minority charge can be accomplished either by active means, via **negative terminal current**, or by passive means, via **recombination**. Normally, both mechanisms occur simultaneously.

The charge contained in the negative portion of the diode turn-off current waveform is called the **recovered charge**.

Minority charges are actively-removed during interval (4).

At the end of interval (4), the stored minority charge in the vicinity of the **junction has been removed**, such that the diode junction becomes **reverse-biased** and is able to **block negative voltage.**

The depletion region **effective capacitance is then charged** during interval (5) to the negative off-state voltage.

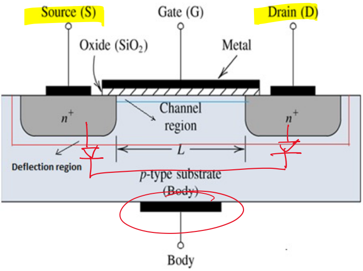
The portion of Q during interval (5) is **charge supplied to the depletion region**, as well as minority charge that is actively removed from remote areas of the diode.

At **the end of interval** (5), the diode is able **to block the entire applied reverse voltage**.

The length of intervals (4) and (5) is the **reverse recovery time t_r**

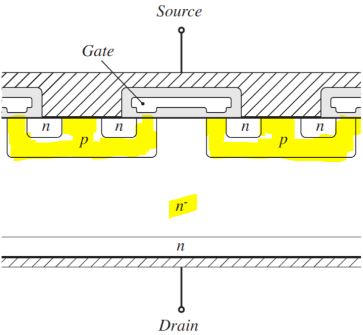
Q_r: reverse recovery charges: diode is very slow!

Power MOSFETs


Source (S)
Gate (G)
Drain (D)
Oxide (SiO_2)
Metal
Channel region
n^+
n^+
L
Deflection region
p-type substrate (Body)
Body

How to make a power MOSFET?

Power MOSFETs

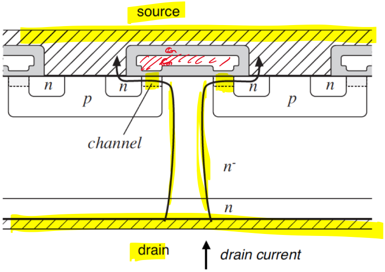

Source
Gate
n
n
p
n
n
p
n^-
n
Drain

- Gate lengths approaching one micron
- Consists of many small enhancement-mode parallel-connected MOSFET cells, covering the surface of the silicon wafer
- Vertical current flow
- n-channel device is shown

Fundamentals of Power Electronics, Robert W. Erickson, Dragan Maksimović

Power MOSFETs

Forward polarization: $V_{gs} > 0$


source
n
p
n
n
p
n
channel
n^-
n
drain
drain current

- p-n^- junction is slightly reverse-biased
- positive gate voltage induces conducting channel
- drain current flows through n^- region and conducting channel
- on resistance = total resistances of n^- region, conducting channel, source and drain contacts, etc.

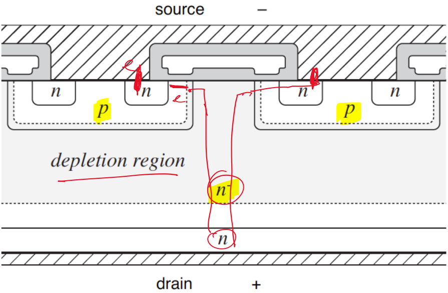
There are no minority carriers to cause conductivity modulation: **MOSFETs are majority carrier devices**

- Breakdown voltage is increased
- On-resistance dominated by resistance of n^- region.

Fundamentals of Power Electronics, Robert W. Erickson, Dragan Maksimović

Power transistors

Reverse polarization: $V_{gs} < 0$

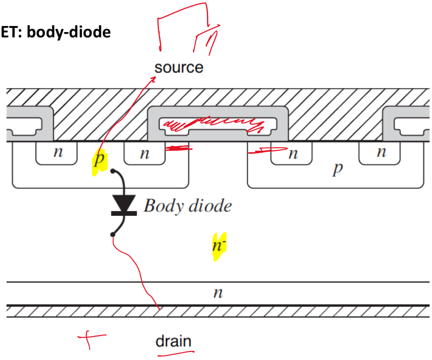

source –
n
n
n
n
p
p
e
e
depletion region
n^-
n
drain +

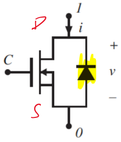
- p-n^- junction is reverse-biased
- off-state voltage appears across n^- region

Polarisation reverse:

p-n and p-n^- reverse-biased: voltage drops across n^- region

MOSFET: body-diode


source
n
p
n
n
p
n
Body diode
n⁻
n
drain
+



Power MOSFET, and its integral body diode

- p-n^- junction forms an effective diode, in parallel with the channel
- negative drain-to-source voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q_r is large

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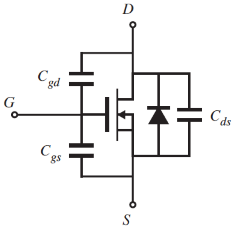
MOSFET: equivalent circuit


D
C_{gd}
G
C_{ds}
C_{gs}
S

- C_{gs} : large, essentially constant
- C_{gd} : small, highly nonlinear
- C_{ds} : intermediate in value, highly nonlinear
- switching times determined by rate at which gate driver charges/discharges C_{gs} and C_{gd}

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \qquad C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$

C_{gd} is small but the voltage is large: so a lot of charges stored